

EURO-DAC 93/EURO-VHDL 93



2

PDAS: Processor design automation system - IEEE Xplore Document In Proceedings of the European Design Automation Conference EURO-DAC93/EURO-VHDL93, pages 130135. IEEE Computer Society Press, 1993. **Formal Methods in Computer-Aided Design: Second International - Google Books Result** the mixed mode interface concerning the analog VHDL is an urgent. 546. 0-8186-4350-1f93 \$3.00 0 1993 IEEE .. Euro-VHDL P1 pp 251-259, September 91. **Synchronous designs in VHDL - IEEE Xplore** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **Computer-aided technique for optimal design of defect-tolerant VLSI** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **Synchronous designs in VHDL - IEEE Xplore Document** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **Sanjiv Narayan - Google Scholar Citations EURO-DAC 93/EURO-VHDL 93 (April 1994 edition) Open Library** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **Features supporting system-level specification in HDLs** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **REGGEN-Test pattern generation on register transfer level - IEEE Euro-Dac93 / Euro-VHDL93: Hamburg Set. 93. European Design Automation Conference e European Conference on VHDL Methods que assistiu e participou** **A framework for macro- and micro-time to model VHDL attributes** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **Technology independent boundary scan synthesis (design flow link to automatic verification methods for VHDL based designs. semantics oriented towards simulation of VHDL de-** 0-81864350-1/93 \$3.00 0 1993 IEEE **Layout-level design for testability rules for a CMOS cell library - IEEE** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #:. Date of Conference: 20-24 Sept. **A net-based semantics for VHDL - IEEE Xplore Document** specification and design using VHDL as the only specification and description 500. 0-8186-4350-U93 \$3.00 0 1993 IEEE .. Design Automation Conference (DAC), pages. 225-230, 1992. Software . In Proceedings of the EURO-VHDL, **State-machine-development-tool for high-level-design entry and** A formal semantics for VHDL based on interpreted Petri nets is defined. Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings

EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. 1993. **A net-based semantics for VHDL - IEEE Xplore** published in the last Euro-VHDL Conference [DeOd]. We defined 0-8186-4350-193 \$3.00 !GI. 1993 Lets define a combinational element as either a VHDL. **Using VHDL for HW/SW co-specification - IEEE Xplore** In Proceedings of the 28th Design Automation Conference, DAC 1991, pages Design Automation Conference, with EURO-VHDL 93, EURO-DAC 1993, **On the modeling and testing of VHDL behavioral descriptions of** The authors compare VHDL with five other specification languages: HardwareC, SDL (Specification and Description Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. **A new mixed mode simulation - IEEE Xplore** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. 1993. **TONIC: A timing database for VLSI design - IEEE Xplore Document** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. **A consistent nonlinear simulation environment based on improved** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. **Interface specification and synthesis for VHDL processes - IEEE** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. 1993. **Formacao Profissional Diversa - INESC-ID** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. **A formal model for coupling computer based system and physical** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. **Implementation of the conception of flexible integration within the** Published in: Design Automation Conference, 1993, with EURO-VHDL 93. Proceedings EURO-DAC 93., European. Article #: . Date of Conference: 20-24 Sept. **Transistor-Level Layout of Integrated Circuits - Google Books Result** Design Automation Conference, 1992., EURO-VHDL92, EURO-DAC92. European, 66-71, 1992 Design Automation Conference, 1993, with EURO-VHDL93.